WHAT IS CLAIMED IS:

1. A semiconductor device, comprising a first DRAM section including a first memory cell having a first capacitance and a second DRAM section including a second memory cell having a second capacitance different from the first capacitance, the first DRAM section and the second DRAM section being provided on the same semiconductor substrate.

2. The semiconductor device of claim 1, wherein an operating voltage of the first DRAM section is higher than that of the second DRAM section, and the first capacitance is smaller than the second capacitance.

3. The semiconductor device of claim 1, wherein a capacitor lower electrode of the first memory cell is provided in the semiconductor substrate, whereas neither of a capacitor upper electrode and a capacitor lower electrode of the second memory cell is provided in the semiconductor substrate.

4. The semiconductor device of claim 1, wherein a capacitor lower electrode of the first memory cell is made of silicon and a surface thereof is not roughened, whereas a capacitor lower electrode of the second memory cell is made of silicon and a surface thereof is roughened.

5. The semiconductor device of claim 1, wherein different materials are used for a capacitor insulating film of the first memory cell and for a capacitor insulating film of the second memory cell.

6. A semiconductor device, comprising a first DRAM section including a first memory cell having a first capacitive element and a second DRAM section including a second memory cell having a second capacitive element, the first DRAM section and the second DRAM section being provided on the same substrate, wherein:

the semiconductor substrate and the first capacitive element are connected to each other by a first plug, and the semiconductor substrate and the second capacitive

element are connected to each other by a second plug; and

different materials are used for the first plug and for the second plug.

7. The semiconductor device of claim 6, wherein a contact resistance between the first plug and the semiconductor substrate is different from that between the second plug and the semiconductor substrate.

8. A method for manufacturing a semiconductor device, comprising the steps of:

successively forming a first capacitor insulating film and a first capacitor upper electrode on a semiconductor substrate in a first memory region, thereby forming a first capacitive element;

forming an interlayer insulating film on the semiconductor substrate, on which the first capacitive element has been formed;

forming a plug connected to the semiconductor substrate in the interlayer insulating film in a second memory region; and

successively forming a second capacitor lower electrode connected to the plug, a second capacitor insulating film and a second capacitor upper electrode on the interlayer insulating film in the second memory region, thereby forming a second capacitive element.

9. A method for manufacturing a semiconductor device, comprising the steps of:

forming an interlayer insulating film on a semiconductor substrate;

forming a first plug and a second plug connected to the semiconductor substrate in the interlayer insulating film in a first memory region and in a second memory region, respectively;

forming a first capacitor lower electrode, which is made of silicon and connected to the first plug, on the interlayer insulating film in the first memory region, and forming a second capacitor lower electrode, which is made of silicon and connected to the

second plug, on the interlayer insulating film in the second memory region;

selectively roughening only a surface of the second capacitor lower electrode; and

forming a first capacitor upper electrode on the first capacitor lower electrode with a first capacitor insulating film interposed therebetween, thereby forming a first capacitive element, and forming a second capacitor upper electrode on the roughened second capacitor lower electrode with a second capacitor insulating film interposed therebetween, thereby forming a second capacitive element.

10. The method for manufacturing a semiconductor device of claim 9, wherein:

a step of removing a native oxide film covering the surface of the second capacitor lower electrode by using hydrofluoric acid is performed between the step of forming the first and second capacitor lower electrodes and the step of roughening the surface of the second capacitor lower electrode; and

the step of roughening the surface of the second capacitor lower electrode includes a step of subjecting the semiconductor substrate to a heat treatment in a silicon-containing gas atmosphere.

11. A method for manufacturing a semiconductor device, comprising the steps of:

forming an interlayer insulating film on a semiconductor substrate;

forming a first plug and a second plug connected to the semiconductor substrate in the interlayer insulating film in a first memory region and in a second memory region, respectively;

forming a first capacitor lower electrode, which is made of silicon and connected to the first plug, on the interlayer insulating film in the first memory region, and forming a second capacitor lower electrode, which is made of silicon and connected to the second plug, on the interlayer insulating film in the second memory region;

forming a first capacitor insulating film made of a first material on the first capacitor lower electrode, and forming a second capacitor insulating film made of a second material different from the first material on the second capacitor lower electrode; and

forming a first capacitor upper electrode on the first capacitor insulating film, thereby forming a first capacitive element, and forming a second capacitor upper electrode on the second capacitor insulating film, thereby forming a second capacitive element.

12. A method for manufacturing a semiconductor device, comprising the steps of:

forming an interlayer insulating film on a semiconductor substrate;

forming a first hole reaching the semiconductor substrate in the interlayer insulating film in a first memory region;

forming a first plug made of a metal film in the first hole;

forming a second hole reaching the semiconductor substrate in the interlayer insulating film in a second memory region;

forming a second plug made of a silicon film in the second hole; and

successively forming a first capacitor lower electrode connected to the first plug, a first capacitor insulating film and a first capacitor upper electrode on the interlayer insulating film in the first memory region, thereby forming a first capacitive element, and successively forming a second capacitor lower electrode connected to the second plug, a second capacitor insulating film and a second capacitor upper electrode on the interlayer insulating film in the second memory region, thereby forming a second capacitive element.